

## VIKASH INSTITUTE OF TECHNOLOGY, BARGARH

## **LESSON PLAN**

		LESSON PLAN		
Semeste	er: 4th	Year: 2025	Course:Btech	
		Sub:COA	Total Credit:3	
Branch : CSE		Sub Code : : RCS4C003		
Name of the Faculty:		: SANJUKTA URMA		
Designation :		Lecturer		
Department :		Computer Science & Engineering		
Session		2024-25		
Recommended Books		Text book:		
		<ol> <li>"Computer Organization and Design: The Hardware/Software Interface", 5th Edition by David A. Patterson and John L. Hennessy, Elsevier.</li> <li>"Computer Organization and Embedded Systems", 6th Edition by CarlHamacher, McGraw Hill Higher Education.</li> </ol>		
		<ol> <li>"Computer Organization and Design: The Hardware/Software Interface",</li> <li>5th</li> <li>Edition by David A. Patterson and John L. Hennessy, Elsevier.</li> <li>Computer Organization and Embedded Systems", 6th Edition by</li> <li>CarlHamacher,</li> <li>McGraw Hill Higher Education</li> </ol>		
		Sl. No.	Lecture No.	Topics to be covered
		MODULE-1		
1	Lecture-01	Functional blocks of a computer: CPU, memory		
2	Lecture-02	Input-output subsystems	1	
3	Lecture-03	Control unit. Instruction set architecture of a CPU–registers,	-	
4	Lecture-04	Instruction execution cycle	-	
5	Lecture-05	RTL interpretation of instructions,	8	
6	Lecture-06	addressing modes	-	
	Locture 07	, , , , , , , , , , , , , , , , , , ,	-	
7	Lecture-07	Instruction set.	4	
8	Lecture-08	Case study – instruction sets of some common CPUs.		
		MODULE-2		
9	Lecture-09	signed number representation, fixed and floating point representations		
10	Lecture-10	character representation	1	
11	Lecture-11	Computer arithmetic – integer addition and subtraction	]	
12	Lecture-12	Ripple carry adder, carry look-ahead adder, e	9	
13	Lecture-13	Multiplication – shift and add,	1	
14	Lecture-14	-	1	
15	Lecture-15	Booth multiplier, carry save multiplier,		
16	Lecture-16	Division restoring and no restoring techniques,	4	
		Division restoring and no restoring reciniques,	_	

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		MODULE-3	
18	Lecture-18	Introduction to x86 architecture. CPU control unit design: hardwired and micro-programmed design approaches	
19	Lecture-19	Case study – design of a simple hypothetical CPU.	
20	Lecture-20	Memory system design: semiconductor memory technologies	
21	Lecture-21	memory organization.	
22	Lecture-22	Peripheral devices and their characteristics: Input-output subsystems	
23	Lecture-23	I/O device interface,	40
24	Lecture-24	I/O transfers–program controlled,	13
25	Lecture-25	interrupt driven and DMA,	
26	Lecture-26	privileged and non-privileged instructions,	
27	Lecture-27	software interrupts and exceptions	
28	Lecture-28	interrupt driven and DMA	
29	Lecture-29	Programs and processes—role of interrupts in process state transitions	
30	Lecture-30	I/O device interfaces – SCII, USB	
		MODULE-4	
31	Lecture-31	Pipelining: Basic concepts of pipelining,	
32	Lecture-32	Throughput and speedup.	
33	Lecture-33	pipeline hazards ,Parallel Processors: Introduction to parallel processors,	
34	Lecture-34	Parallel Processors: Introduction to parallel processors,	7
35	Lecture-35	Concurrent access to memory and cache coherency	
36	Lecture-36	CPU Basics: Multiple CPUs, Cores, and Hyper-Threading,,	
37	Lecture-37	Introduction to Multiple-Processor Scheduling in Operating System.	
		MODULE-5	
38	Lecture-38	Memory organization: Memory interleaving	
39	Lecture-39	concept of hierarchical memory organization	
40	Lecture-40	concept of hierarchical memory organization	
41	Lecture-41	cache memory	
42	Lecture-42	cache size vs. block size,	
43	Lecture-43	mapping functions,	
44	Lecture-44	replacement algorithms	
45	Lecture-45	write policies	8

## Signature of Faculty Member

## Signaturer Of HOD